Remarks

In the Final Office Action dated November 25, 2009, the following rejections were indicated: claims 1, 2, 5, 6, 14-16 and 21 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy (U.S. Patent No. 6,233,178) in view of Iwahashi (U.S. Patent No. 4,247,918); claims 3, 7-9, 11, 17 and 20 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 reference further in view of Guliani (U.S. Patent No. 6,366,497); claims 4 and 10 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 and '497 references and further in view of Takahashi (U.S. Patent No. 6,639,849); and claims 12-13 and 18-19 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 and '497 references and further in view of Kurihara (U.S. Patent Pub. 6,791,880). Applicant respectfully traverses all claim rejections, and in this discussion set forth below, does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

The Examiner's response to arguments section suggests a lack of understanding of the relevant technical art and the teachings of the references being relied upon in the rejection. For instance, the Examiner alleges that "(a) floating gate is a charge trapping device else it would not be a non-volatile memory device." The third paragraph of Applicant's specification explains that this is not the case and explicitly defines a charge trapping device as not including floating gate devices. Thus, even were the Examiner to present evidence in support of another definition (which has not yet been presented), the M.P.E.P. and case law prohibit interpretations that are inconsistent with the invention disclosure. (*See, e.g.*, M.P.E.P. § 2111.01 "Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim. *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999)"). Accordingly, the rejection is invalid for relying upon a claim interpretation that is both lacking any evidentiary support and that is inconsistent with Applicant's specification.

In another instance, the Examiner states that "The Iwahashi reference is merely to teach that the relationship between erasing to a 0 or a 1 is well known in the art and that it would be obvious to swap the roles of charging and discharging accordingly." This, however, fails to recognize that the teachings of the '918 reference are unrelated to the

failings of the cited references. The relevant claim limitations are directed toward charge and discharge states rather than logical '0' or '1' values. As Applicant's previous response attempts to explain, the relied upon portions of the '918 reference do not appear to correspond to any change in the underlying physical/electrical properties of the device. Instead, they represent two different logical interpretations of the same signal. In a first implementation a charge state could represent a logical "1" and a discharge state could represent a logical "0." In a second implementation a charge state could represent a logical "0" and a discharge state could represent a logical "1." In either case, the underlying memory device is unchanged. Thus, the failings of the primary reference are not cured. In particular, switching logical ones or zeroes does not change the underlying charge states and function of the device. That is to say that the required erasure and programming step for a write operation does not change simply because the logical values are swapped. Thus, the device of the '918 reference would still perform block erasures in the exact same manner (relative to charge and discharge states) regardless of how logical ones or zeroes are assigned. Accordingly, the proposed modification would not correspond to the claim limitations.

The Examiner continues not to afford any consideration to the fact that the '178 reference relates to floating gate memory, whereas Applicant's claimed invention is directed towards charge trapping memories. In this respect, Applicant's specification explains that the inventor observed that charge trapping memories exhibit different characteristics from floating gate memories (*see, e.g.*, Applicant's specification, page 2:16-20), and that 'program induced degradation' does not exist for charge trapping memory devices (*see, e.g.*, Applicant's specification, page 15:28-16:5). In contrast, the '178 reference expressly teaches that the problem being addressed by the '178 reference is due to excess charge buildup. Thus, the proposed combination, based upon the primary '178 reference, not only fails to correspond to the claim limitations but also expressly teaches that charging is a problem to be avoided. Since Applicant's specification is the only art of record that explains and teaches that charging of charge trapping memory devices is beneficial, it is impermissible for the Examiner to allege obviousness of this recognition especially where the cited references expressly lead the

skilled artisan in the opposite direction. This is supported by numerous rules and legal holdings, some of which are explained in more detail hereafter.

The stated purpose of the '178 reference is to precondition the cells before an erasure ever occurs to specifically avoid charging an already charged cell. The '178 reference explains that this is done to mitigate stress buildup due to erasures (Col. 5:39-40). The Examiner's proposed modification of the '178 reference would result in charging already charged cells. As such, it is impermissible to modify the '178 reference in a manner that defeats the express and primary purpose of avoiding charging already charged cells. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P. 2143.01 citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As consistent with the above, the '178 reference also teaches away from the claimed invention. The discharging and subsequent charging steps of the '178 reference are described in the reference's Abstract and cited column 4, in which flash memory devices are first preconditioned by discharging cells, prior to charging the cells. The erasing step in the '178 reference is further described at column 5:1-3, which indicates that "[d]uring the erase step 320, all cells 120 within a sector are erased, setting cells 120 within the sector to their charged state" (*i.e.*, the cells are erased by charging). This is consistent with the discussion at page 3 of the previous Office Action, which states that the '178 reference "discharges cells as taught in Col 4 lines 43-45" as a preconditioning (first) step.

Importantly, the background of Applicant's specification explains that there are various issues with the '178 reference's charging and discharging approach (*see, e.g.*, Applicant's specification, page 2:7-22). Specifically, the '178 reference's preconditioning step involves discharging that may result in discharging an already discharged memory cell, which can deteriorate the cell. The claimed invention addresses such problems (*see, e.g.*, Applicant's specification, page 2:23-26) and presents a memory control solution with results that are clearly different than those in the '178 reference. Accordingly, since the '178 reference teaches a memory management approach that

causes the problems noted in the background of the instant application, the reference actually teaches away from the asserted combination of references.

The M.P.E.P. and the applicable U.S. Supreme Court law requires that the claim be considered "as a whole" (35 U.S.C. §103(a)), while taking into consideration the problem(s) being addressed by the claimed invention and any unexpected results. Thus, the Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), and stated that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). Accordingly, the '178 reference not only fails to disclose or contemplate the claimed invention, it further teaches away from the claimed invention.

In view of the above, the cited portions of the '178 reference fail to disclose, teach or suggest limitations in both of independent claims 1 and 5. As the rejections of claims 2-15 and 21 rely upon the misapplied portions of the '178 reference, these rejections are improper and should be removed.

In view of the above, Applicant believes that further discussion of the Section 103 rejections is unnecessary. However, Applicant submits that the proposed combinations of references cannot stand, as the resulting structure would not correspond to the claimed invention (per the above), and would render the '178 reference inoperable for its purpose (as relevant to replacing its discharging/charging steps with the steps as claimed), which contradicts the M.P.E.P. and relevant law. Applicant therefore submits that the Section 103 rejections are also improper for these reasons.

Applicant further notes that the rejection of claims 8 and 17 does not establish a *prima facie* case of obviousness. The cited portion of the '497 reference simply teaches that the reference cell can be used for programming or erasing configurations, but it does not teach that the reference cell is actually programmed and erased for a block-programming and block-erasing of the non-volatile memory devices in the array.

Applicant directs the Examiner to Applicant's specification beginning at page 17, which explains the differences between floating gate memories and charge trapping memories and provides evidence of the nonobviousness of this aspect (*e.g.*, due to aspects taught by Applicant's specification and not otherwise recognized by the references cited in the rejection of claims 8 and 17).

Moreover, the Examiner's inherency argument either relies upon an improper interpretation of the relevant limitations or is unsupported and invalid. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" M.P.E.P. § 2112 citing to *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted). Thus, the existence of a single implementation that does not correspond to the alleged inherent aspect invalidates any argument of inherency. The primary '178 reference does not respond to a block erase request by programming before erasure. This sequence of programming and erasure is not inherent as the erasure could be (and is taught to be) implemented without first programming. Accordingly, the rejection is *prima facie* invalid.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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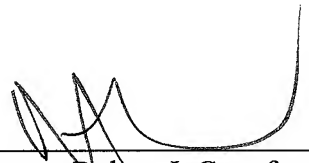
By: 

Name: Robert J. Crawford
Reg. No.: 32,122
Shane O. Sondreal
Reg. No.: 60,145
651-686-6633
(NXPS.330PA)